



ML4039 BERT User Operation Manual

www.multilaneinc.com

ML4039

4 Lane 8-15 & 21-30Gbps BERT



The screenshot displays the ML4039 BERT software interface. At the top, the status bar shows: Help, Internal Loopback (Disabled), SaveLoad, Calibration, APIRev: 2.6, FWRev: 2.6, BoardID: 4319, BoardSN: 210DF00011092. On the right, TX LOCK and RX LOCK indicators are shown for channels CH0 (24°C), CH1 (24°C), CH2 (22°C), and CH3 (22°C).

Configuration Table:

Jit	TX Pattern	RX Pattern	Amplitude	TX Skew	PM	AM RJ	Error-Insr
Ch 0	PRBS 7	PRBS 7	0	1.00	1	0	Disabled
Ch 1	PRBS 7	PRBS 7	0	1.00	0	0	Disabled
Ch 2	PRBS 7	PRBS 7	207	1.00	0	0	Disabled
Ch 3	PRBS 7	PRBS 7	206	1.00	0	0	Disabled
all ch	-	-	-	-	-	-	Disabled

BER Graph:

The BER graph shows BER on a logarithmic y-axis (from 10⁻¹ to 10¹) versus Acquisition on the x-axis (from 0.0 to 1.2). The legend indicates four channels: Ch0 (black), Ch1 (green), Ch2 (red), and Ch3 (purple). The graph area is currently empty.

Configuration Panel (Left):

- IP: 172.16.102.221
- Clock Configuration: Internal selected, Rate: 10 Gbps, Ref: 250 MHz
- BER Analysis: Real Time BER selected, Count (25 Kb): 10, Multi Acquisition: 1
- Continuous mode selected, BER: 10, Bits Count (Gb): 10, Timer: 00 d 00 h 00 m 30 s
- Channels CH0, CH1, CH2, and CH3 are checked.

Buttons: Disconnect, Apply, Start, Save Results, Done.

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Windows GUI Version v.3.0.r3784
API Version 2.7
Firmware Version 2.6

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General Safety Precautions

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the General Safety Summary in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Only use the power cord specified for this product and certified for the country of use.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers.

Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures.

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Symbols and Terms in this manual. These terms may appear in this manual:

⚠ CAUTION: *Caution statements identify conditions or practices that could result in damage to this product or other property.*

⚠ CAUTION: *Provide adequate cooling. Provide adequate cooling to the board to avoid damaging any part of it specifically for the ATE version of the board. Refer to the power section to know the power dissipation values*

Preface

This is the user operation manual for the [ML4039](#). It covers the following information:

- Describes the capabilities of the instrument: how to install it and its software
- Explains how to operate the instrument for: Pattern generation, Error Detection; how to control the clocking system, inputs/outputs and all the available measurements
- Lists the specifications

Contact MultiLane SAL

MultiLaneSAL is an engineering services company and an OEM supplier of specialty test and communication equipment for the semiconductor and optical transport industries. Multilane delivers ultra-compact test instruments of the highest value and performance for high speed communication and signal integrity applications. The Company has a large engineering team and a fully equipped lab with state of the art equipment, having recently moved to a 6000sq foot facility in **Houmal Technology Park (HTP)**.

MultiLaneSAL customers can leverage great flexibility and capability in product customization thanks to our team in depth expertise in high speed I/O, Signal Integrity, and access advanced development and test tools. MultiLane has the resources and know-how to meet customer's product development and design requirements. Our R&D has a proven track record in delivering leading edge products and development tool kits to the Automated Test market while applying the production processes to deliver high quality products on schedule and within budget.

MultiLaneSAL's team is composed of experienced and disciplined engineers offering products and turnkey solutions of modules and systems for high speed IO, Signal Integrity, SOC development and optical communication from verbal requirements (Architecture, PRD, HW/FW/SW design implementation and characterization).

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Product Description

This chapter describes your instrument, operating under Windows.

- *Installation* shows you how to configure and install the instrument, as well as how to install the system software included with the product.
- *Incoming Inspection* provides a procedure for verifying basic operation and functionality
- *Accessories and Options* lists the instrument options available and the standard and optional accessories for this product.

Model and Package Content

This manual supports the instrument **ML4039 (cPCI & ATE)**

Hardware Packages

ML4039 (cPCI & ATE): Four-Channel 30 Gbps BERT, reference clock output, recovery clock output (**Optional**), external reference clock input (**Optional**)

User Guide Manual

Manual containing user operation guide, software installation and start up procedure.

Software package and documentations:

- Main **ML4039** GUI.
- USB driver. The Ethernet interface is controlled through the API version 2.0 that includes the Ethernet package.

Overview

ML4039 is a low cost, simple to use, fully integrated, ultra compact, USB/Fast Ethernet controlled instrument that combines the functions and features of a signal generator, bit error-rate tester and data analysis system with Post Emphasis and Pre Emphasis capabilities. It is also verified to fit in common ATE platforms.

Moreover, MultiLane offers the **ML4039** instrument in a cPCI card format that fits into the **ML4000** MultiLane Signal Integrity Analyzer 6U cPCI Chassis.

Key Features

- Available in ATE and cPCI form factors
- 8.5-15 and 21-30 Gbps data rates
- External reference clock input
- Low intrinsic jitter < 270 fs
- Automated J2/J9 measurement
- Integrated synthesizer
- Eye contour measurement
- Jitter Tolerance measurements (ML407 required)
- Intuitive comprehensive GUI
- Window and Linux API functions
- Repeatable traceable measurements

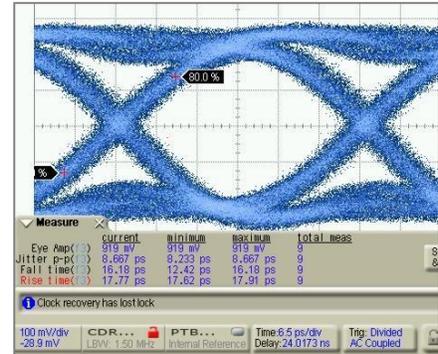


Figure 1: Eye Display

BER and measurement suite

- Low cost simple to use 4 channel BERT
- Supports all basic BERT functions
- Complete BERT measurement capability (eye contour and bathtub curve)
- 6 dB pre-emphasis
- 10 dB CTLE calibration

Target Applications

- Interconnect testing, CFP2, CFP4, QSFP28
- Backplane testing
- Interference and crosstalk testing
- Receiver sensitivity testing
- Receiver jitter tolerance testing
- Equalizer characterization
- Electro-optical module testing
- Electrical stressed eye testing for 100 Gbps Ethernet, MLD/CAUI application, OIF CEI-28G-VSR, CPPI-4, CAUI-4, 32G Fiber Channel chip to module

Electrical Specifications

Generator Data Out		
Bit Rates	8-15 and 21-30Gbps	
TX Amplitude Differential	200-800mV	
Data Format	NRZ	
PRBS Patterns	7, 9, 11, 15, 23, 31, sinusoidal and user Pattern 40 bits	
TX Amplitude Adjustment	200mV	
Rise/ Fall Time (20–80%)	14 pS	
Pre-Emphasis	6 db	
Pre-Emphasis Resolution	10 steps	
Equalizing Filter Spacing	1UI	
Reference Clock		
System Clock	Clock Out	Rate/16 (Rate between 8-15) Rate/40 (Rate between 21-30)
	Clock input	Rate/16 (Rate between 8-15) Rate/40 (Rate between 21-30)
Stress Jitter Generator		
Random Jitter (rms)	0.4ps	
Deterministic Jitter @ 25G	2ps	
Error Detector		
Data input amplitude	110-1050mV Differential	
Maximum Input	1200mV Diff	
Vertical Scan Resolution	8 bits	
Phase Scan Resolution	7bits	
Phase margin	5ps	
Input Sensitivity	25mVpp	
Input CTLE Dynamic Range	10dB	
Return Loss		
Output Return Loss up to 10GHz	-15 dB	
Output Return Loss	-8dB	
Power Requirements		
	21.5 Watt	
Connectors		
TX/RX and clock connectors in cPCI	2.92 K Connectors	
TX/RX and Clock Connectors in ATE	SMPM-RA	
Electrical Specifications		
CLKIN Min Differential Voltage	0.4 V	
CLKIN Max Differential Voltage	1.0 V	
CLKOUT Min Differential Voltage	1.1 V	
CLKOUT Max Differential Voltage	1.6 V	

Product Software

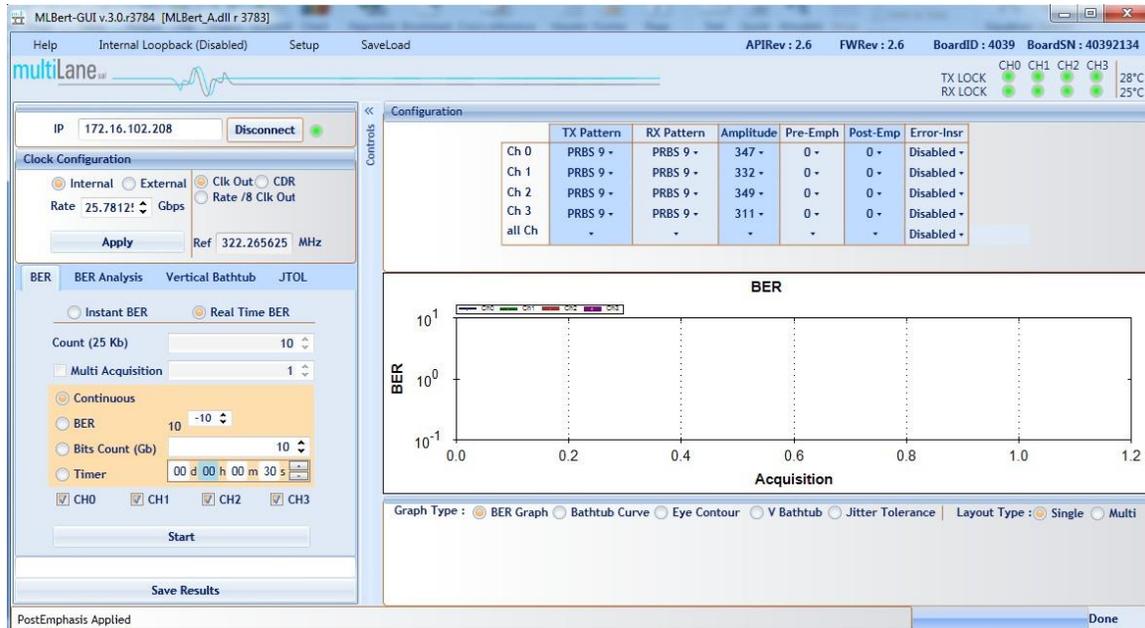


Figure 2: ML4039BERT GUI

The instrument includes the following software:

- [ML4039 GUI.](#)
- [MultiLane ML4039 USB driver.](#)
- [ML4039 ETH Configuration Software.](#)

Instrument GUI runs on Windows XP (32/64 bit), Windows 7 and 8.

NOTE. These applications requires the Microsoft .NET Framework 3.5.
 If the Microsoft.NET Framework 3.5 is needed, it can be downloaded through this link:
<http://download.microsoft.com/download/2/0/e/20e90413-712f-438c-988e-fdaa79a8ac3d/dotnetfx35.exe>.

For more products updates, check the following webpage:

www.multilaneinc.com/products.html

Minimum PC Requirements

The Windows PC properties for the [ML4039 GUI](#) application must meet the following specifications:

- Windows XP SP3 or greater
- Minimum 1 GB RAM
- 1 Ethernet card to establish connection with the device
- USB Connector
- Pentium 4 processor 2.0 GHz or greater
- .NET Framework 3.5 sp1

NOTE. *It is recommended to connect the BERT via Ethernet to one PC only to prevent conflict from multiple user commands.*

Instrument Ports

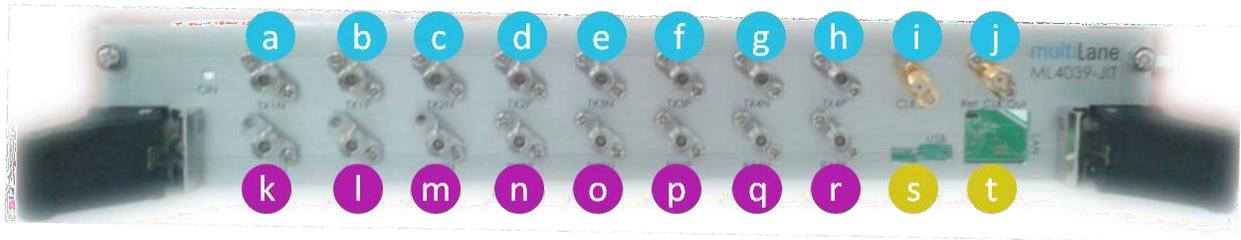


Figure 3: ML4039 cPCI Front Panel

	Port Name	Description
a	TX1N	Negative TX Channel number 1 Amplitude range: 100-1600mV Differential. Bit rate 8.5-15 & 20-30 Gbps – Electric interface (same for all the TX channels)
b	TX1P	Positive TX Channel number 1
c	TX2N	Negative TX Channel number 2
d	TX2P	Positive TX Channel number 2
e	TX3N	Negative TX Channel number 3
f	TX3P	Positive TX Channel number 3
g	TX4N	Negative TX Channel number 4
h	TX4P	Positive TX Channel number 4
i	Clock In	(Optional) Reference Clock Input, input values should be: <ul style="list-style-type: none"> ▪ Rate/16 for Rate between 8-15 ▪ Rate/40 for Rate between 21-30
j	Ref CLK-Out	(Optional) Recovery Clock Output: is the clock recovered from input data signal
k	RX1N	Negative RX Channel number 1 Amplitude range: 100-1200mV. Bit rate 8.5-15 & 20-30 Gbps – Electric interface (same for all the RX channels)
l	RX1P	Positive RX Channel number 1
m	RX2N	Negative RX Channel number 2
n	RX2P	Positive RX Channel number 2
o	RX3N	Negative RX Channel number 3
p	RX3P	Positive RX Channel number 3
q	RX4N	Negative RX Channel number 4
r	RX4P	Positive RX Channel number 4
s		Mini-B USB port
t		RJ 45 port

Table 1: ML4039 cPCI Ports

Installation

This chapter covers installation of the instrument, addressing the following topics:

- System Start-up
- How to connect to the instrument

Note: for windows vista, 7, and 8 users always run the GUI as administrator

System Start-up

To use the **ML4039 GUI** under Windows XP, Windows 7 and 8, it is important that the correct start-up sequence is followed:

- Make sure you have Microsoft *.NET Framework 3.5* installed. If not installed, refer to the Note in the [Product Software](#) section.
- Install the **ML4039** software.
- After installation, open it with a double click on the software icon or from your PC main menu.
- A new window will appear titled **ML4039**; this is the main software interface.
- The board is now powered up (the green Led on the front panel is turned on).
- To connect to the instrument:

Connect through Ethernet:

Connect the PC to the front panel via the RJ45 connector located on the front panel through an Ethernet cable to be able to control it.

In order to connect via Ethernet the IP address of the board is required.

To learn more options on how to connect the Ethernet cable go to the section [Connect through an Ethernet Cable](#).

- Note that no drivers are required; you only have to know the current board IP address, you need to enter it in the text box next to the **IP** label shown in the below picture, then click on the **connect** button.

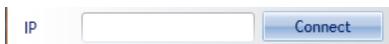


Figure 4: Connect Via Ethernet

- You are now connected.
- Once connected, the **Connect** button turns into **Disconnect**.
- To make sure that you are connected, you can also ping your device.
- To change the IP address of the board, you need to install the USB drivers (refer to section [USB Driver Installation](#)).
- Install the Ethernet configuration software that allows you to read, write the **IP** address, **Mask** and **Gateway** of the instrument.

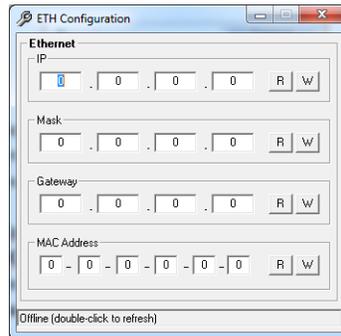


Figure 5: Ethernet Configuration

The instrument is now powered up and connected through the right IP address. Next, you need to configure the signal generated.

Line Rate Configuration

- Write the bit rate value next to the **Line Rate** label. The value entered must be in between 8.5-15 & 21-30 Gbps per lane.
- Press **Apply** to save the value.
- **Ref** will be automatically generated indicating the **Ref CLK-Out** that will be generated by the **ML4039**
- In case the clock is **External** “inserted to the **ML4039**”, values of **Ref-CLK-In** should be the following in order for the signal to be generated properly:
 - If the Revision is **RevA**:
 - Clock = LineRate/16, for LineRate between 8 -15 Gbps
 - Clock = LineRate/40, for LineRate between 21-30 Gbps
 - If the Revision is **RevB**:
 - Clock = LineRate/32, for LineRate between 8 -15 Gbps
 - Clock = LineRate/80, for LineRate between 21-30 Gbps
- **CDR** will have the value of recovered data clock from the input data signal. Recover Clock output can be changed by either selecting to divide the rate by 8 or 16.
- If the Revision is **RevA** the Clock is **625** on low and high rate.
- If the Revision is **RevB** the Clock is **312** on low and high rate.
- **Rate/8 Clk Out** is used for Precision Time Base.

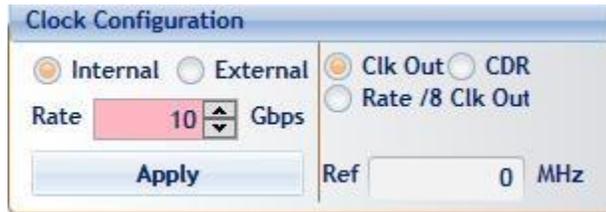


Figure 6: Line Rate Configuration

PRBS Pattern Configuration

- In the **PRBS Configuration** group box, select the pattern required; the available patterns are 7, 9, 15, 23, 31 and sinusoidal in addition to the 40 bits user pattern. TX Pattern tab is used for Configuring Generated signal, RX Pattern tab is used for pattern verification
- To use the **User defined** capability, first select it from the **Pattern** combo box list, then in the text box specified for the **User Defined** write the sequence of bits you want.
The sequence of bits should be in **Hexadecimal** only (16 bits length), ie FF, and then click the Set button.
- To make the TX off, choose the **TX OFF**
- In case the test engineer wired the positive TX channel to the negative RX channel by mistake, the software can compensate for this error by clicking on the invert button.

The specified generator now starts generating a clean signal. If you would like to inject jitter to the signal generated to start shaping the eye diagram, you have to adjust the slide bars existing in the Eye Shaping group box (refer to the section **Eye Shaping**).

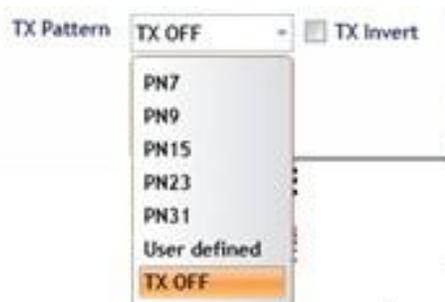


Figure 7: PRBS Channel Configuration

PRBS Pattern Verification

PRBS Verification option checks if the data received at RX is recognizable by the [ML4039](#)

- In case the User manually selects the pattern and checked the invert button, the LED indicates that the channel is locked by turning green. Channel will be locked if the data received at RX matches the selected pattern
- If the user selects **Automatic Verification**, the software will try to detect the received signal pattern and if it is inverted; upon success it will show the result and the LED will indicate that the channel is locked.



Figure 8: PRBS Verification

Eye Shaping

This instrument includes 3 sliders to shape the form of the eye diagram, amplitude, Pre-emphasis and Post-emphasis. All slider values and other configurations are saved in the EPROM:

- Amplitude: TX output amplitude is between 0mV and 1000mV.
- Pre Emphasis:TX output Pre-emphasis amplitude value could be changed from 0 to 20%.
- Post Emphasis:TX output Signal Post-emphasis amplitude value could be changed from 0 to 35%.

Amplitude	Pre-Emph	Post-Emp
0 ▾	0 ▾	5 ▾
0 ▾	0 ▾	5 ▾
194 ▾	0 ▾	5 ▾
0 ▾	0 ▾	5 ▾

Figure 9: Eye Shaping Sliders

Error Insertion

Error-Insr tab allows configuring signal error insertion. **Rate** select list allows the user to choose the amount of error bits. Rate will vary between 1 and 40 bits.

Continuous checkbox allows continuously inserting error to the generated signal.

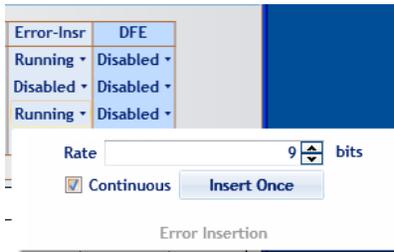


Figure 10: Error Insertion

CTLE Configuration

CTLE Tab allows the user to select the equalization level; CTLE varies from 0 to 10 dB to compensate for cable loss from the DUT to the BERT and to de-embed the system losses.

The auto adapt selects the best CTLE mode

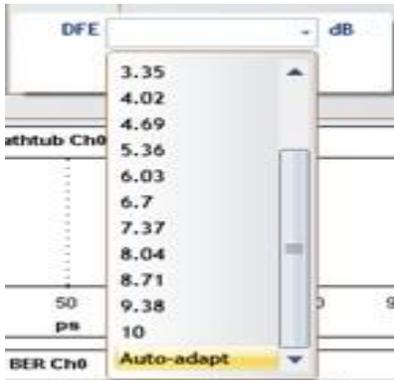


Figure 11: DFE Configuration



In GUI versions 3 release 3784 and above, the CTLE is accessible from the menu bar under Help.

Bit Error Ratio Reading

To be able to start BER measurements, the instrument ports should be in the loopback mode, which means TX port should be connected to the RX port and the **Start All Channels** button must be selected.

To monitor the BER function, we have dedicated an LED to make sure it is locked.

- If the LED is green that means the RX is locked to the incoming data.
- If the LED is red that means the RX is not locked to the incoming data, which means there is a possibility that the cables are not connected correctly, thus try the invert function at the TX and RX sides; if the problem persists check the connections of your cables. The patterns of the Detector are automatically modified when you change the generator pattern value.

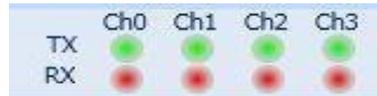


Figure 12: Channels' LEDs

BER

BER test has the following configuration:

Count (25kbit): Number of packets to be collected

Repeat Count: if selected it allows you to choose the number of acquisitions.

The measurements will be for the preceding configuration.

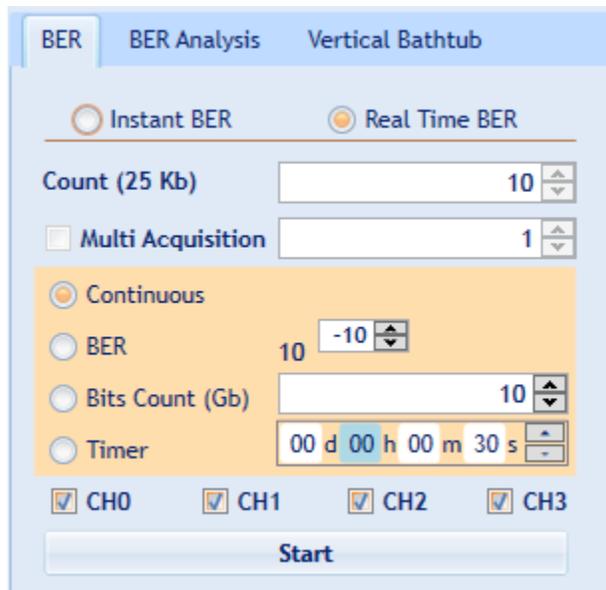


Figure 13: BER Configuration

Real Time BER

This feature allows the BERT to collect Real Time BER.

Configuration

Count (25kbit): Number of packets to be collected.

Repeat Count: if selected it allows you to choose the number of acquisitions.

Continuous BER: the BER value is repeated after each set the packet counts.

BER: The BER test will run till it reaches the amount of BER selected.

Timer: The BER test will run for the specified amount of time.

BER Graph

Plots BER values collected on the graph

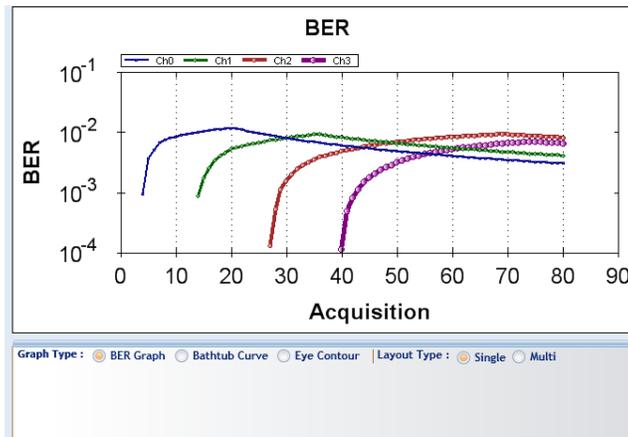


Figure 14: BER Graph

Jitter Tolerance Test



Requires GUI v.3.0.r3784 and above.

Requires an ML407 as external Clock Source with SJ

Our user friendly JTOL tool, allows the user to perform automatic jitter injection for the stressed input applications and for characterization. This tool is featured in the BERT GUI (v.3.0.r3784 and above, MLBert_A.dll r 3783). The tool needs MultiLane' ML407 clock synthesizer (up to 60 MHz) for multi-UI sinusoidal jitter generation and the ML4039 or ML4039-JIT.

This option facilitates 10/40/100Gbps stressed input compliance testing.

If you have an ML4039, you can use it to test your DUT's tolerance to Sinusoidal Jitter by either letting the GUI execute the test automatically according to the limits specified for

CAUI4 or XLAUI4, or by self-defining the frequencies at which the test should be executed and the pass/fail criteria.

With the ML4039-JIT, you can do full Stressed receiver tolerance since the instrument allows you to inject calibrated RJ and BUJ prior to launching the JTOL test. By doing this one would test for BER against a predefined mixture of different jitter components.

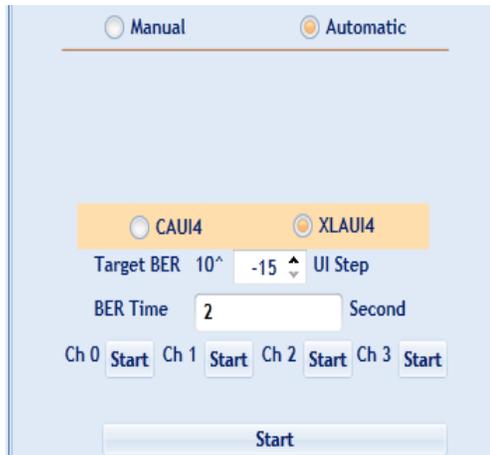


Figure 15: JTOL GUI interface

Modes of operation for the JTOL

Two modes of operation are featured and both require the clock synthesizer's input.

Automatic mode:

Features two masks, CAUI4 for high rate (25.78125Gbps) and XLAUI4 (10.3125Gbps) for low rate. Each test is performed based on the IEEE802.3bm- 2015 standards for high rate and IEEE802.3ba-2010 for low rate.

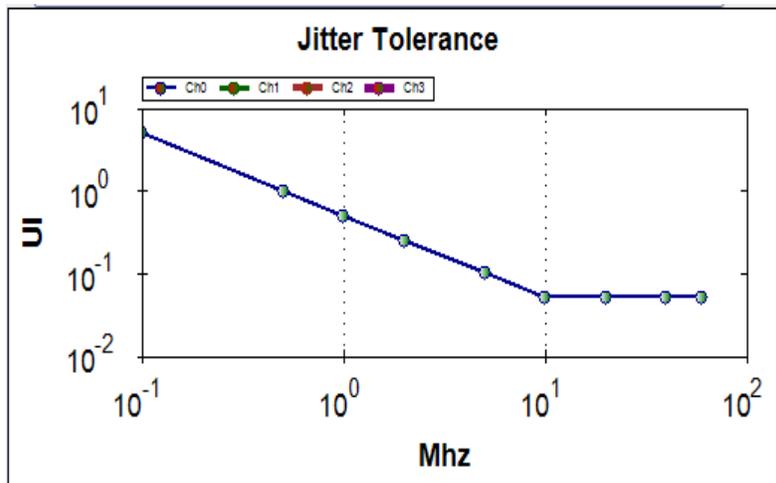


Figure 16: Automatic Mode graph

Manual mode:

The user can choose the desired frequency at which the sinusoidal jitter is generated, also specifying the desired UI interval.

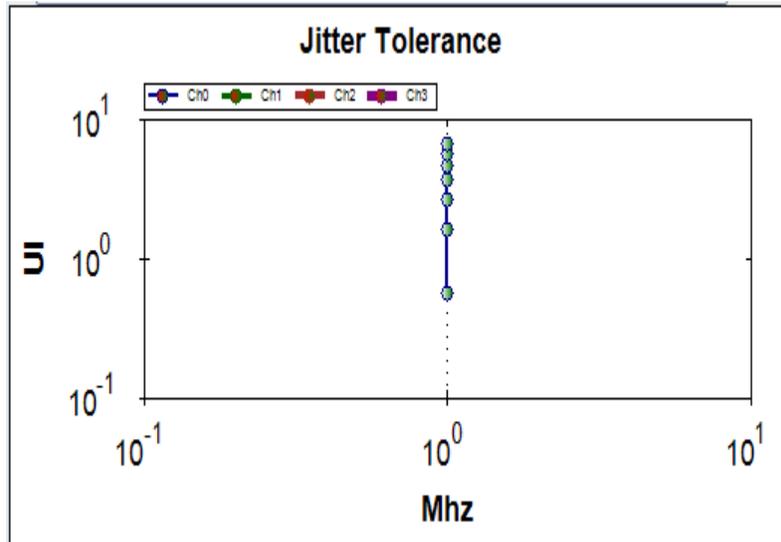


Figure 17: Manual Mode graph

Multi channel JTOL

The JTOL test can be performed simultaneously for 4 channels at a time, and indicates whether the test Fails or Passes.

When the test is performed in automatic mode, the results indicate the channel being tested, frequency at which the test being executed, BER level and the Verdict indicating whether the test Passes or Fails. The results can be saved for later analysis.

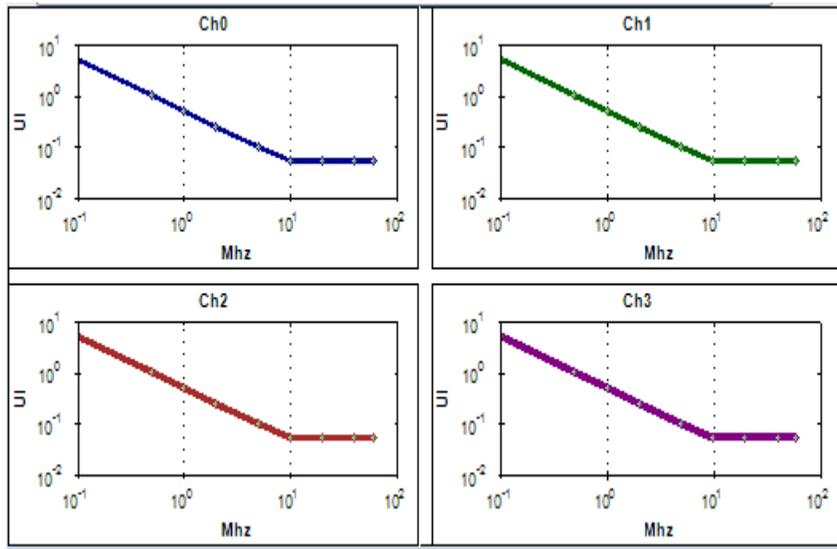


Figure 18: Multi channel Automatic JTOL

Channel	Freq	BER	Verdict
Ch0	0.1	0.00e+00	Pass
Ch1	0.1	0.00e+00	Pass
Ch2	0.1	0.00e+00	Pass
Ch3	0.1	0.00e+00	Pass

Save Results

Figure 19: Automatic mode final results

Regarding the manual option, the same results are displayed with the UI-sinusoidal jitter being injected as well.

Manual Automatic

Frequency MHZ
 Start UI
 Finish UI

Target BER 10[^] UI Step

BER Time Second

Ch 0 Ch 1 Ch 2 Ch 3

Channel UI	BER	Verdict
Ch0	0.562 0.00e+00	Pass
Ch1	0.562 0.00e+00	Pass
Ch2	0.562 0.00e+00	Pass
Ch3	0.562 0.00e+00	Pass

Figure 20: Manual Mode displayed results

Bit Error Ratio analysis

The Bathtub Plot

A viewpoint of jitter is provided by a *bathtub plot*, so named because its characteristic curve looks like the cross section of a bathtub. It is a graph of BER versus sampling point throughout the unit interval. It is typically shown with a log scale, which illustrates the functional relationship of sampling time to bit error ratio. Also the deep eye width can be entered to get the BER level.

When the sampling point is at or near the transition points, the BER is 0.5 (equal probability for success or failure of a bit transmission). The curve is fairly flat in these regions, which are dominated by deterministic jitter mechanisms.

As the sampling point moves inward from both ends of the unit interval, the BER drops off precipitously.

These regions are dominated by random jitter mechanisms and the BER is determined by the sigma of the Gaussian processes producing the random jitter. As expected, the center of the unit interval provides the optimum sampling point. Note that there is BER measured for the middle sampling times.

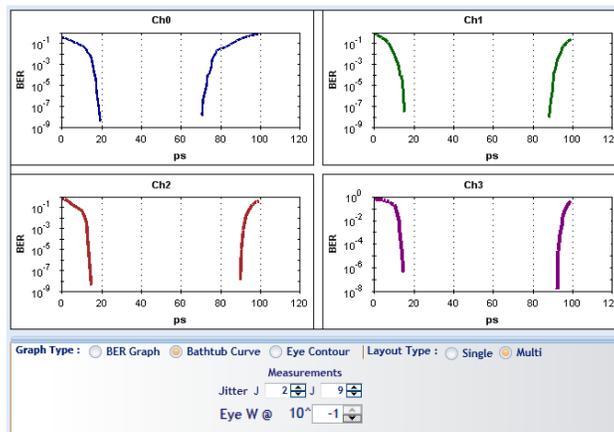


Figure 21: Bathtub Graph

Plotting the points on a graph of BER versus sampling location in time results in a curve that resembles the cross section of a bathtub, hence the term bathtub curve. A bathtub curve can be created either by software extrapolation from voltage over time measurement done by an oscilloscope, or by actually sampling the bits as done by a BERT.

For development engineers, the final proof of performance of a component or subsystem is the direct measurement of BER at optimized timing and threshold levels employing error detection on every transmitted bit. However the speed of the BER measurement is a function of the BER to be measured and the desired statistical confidence factor for the result.

Bathtub configuration

To run the bathtub you should set the following configuration:

Target BER: Select which level the Bathtub will reach. Upon selection, estimation of the time will be given.

Full sweep: Read the BER at every point and allow the user to choose the start and stop time for the scan (time in mS).

You can select a channel at a time to measure the Bathtub.

Dual Dirac: Doesn't allow the user to choose the start and stop time for the scan



Figure 22: Bathtub Configuration

Jitter measurements

J2 and J9 is a measure of the eye width at 2.5×10^{-2} and 2.5×10^{-9} .

J2 gives a measure of the DJ.

J9 gives a measure of the RJ.

The [ML 4039 GUI](#) allows BER Level selection for measurements.



Figure 23: Jitter Measurements

Eye Contour

Eye Contour Configuration

To run the Eye Contour you should set the following configuration:

Accumulated: Select the number of data acquisitions. Upon selection, estimation of the time will be given.

You can select a channel at a time to do the Eye Contour measurements.

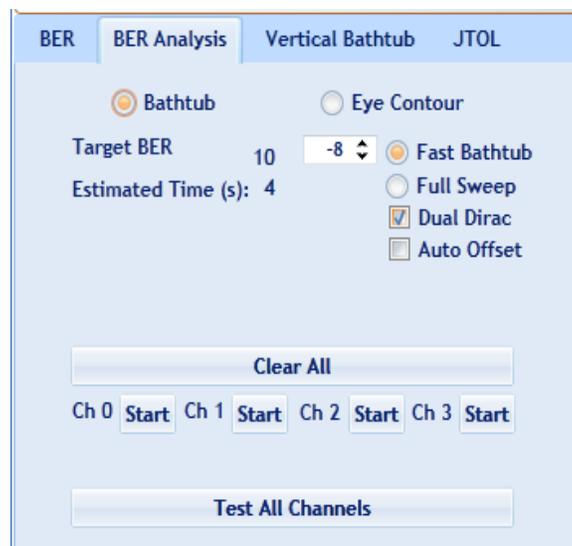


Figure 24: Eye Configuration

Eye Contour measurements

The eye opening is a key characteristic of a device. The BER is displayed as a function of sampling delay and sampling threshold.

Bit Error Rate Contour Measurement is part of the Physical Layer option. This analysis computes the bit error rate around the perimeter of the eye opening and fits these results to the expected bit error rate response curves predicted by additive noise. The depth of the contours can then be extrapolated to lower levels than the actual measurement would allow.

BER contours are used to identify how much headroom may be present in a system after considering the amount of decision-point variation that might occur.

You can press the Eye Scan button to draw the overall eye contour.

In case of single channel Select Offset checkbox will allow to specify a point to read Bathtub and BER in range of picosecond X-axis and millivolt Y-axis.

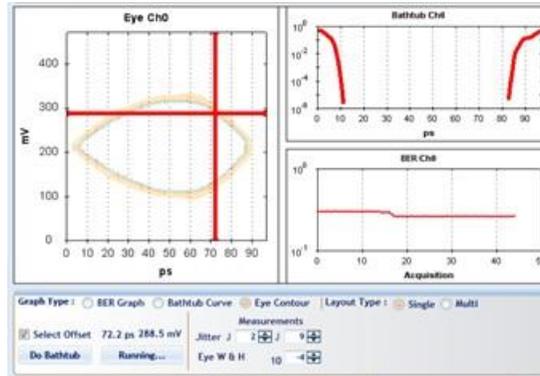


Figure 25: Single Channel Eye Contour

Do **Bathtub** button displays the Bathtub curve and shows Jitter measurements.

Do **BER** button displays BER graph and shows BER results.

These featured are not applicable in 4-Channel mode; the graph will display 4 Eye contour.

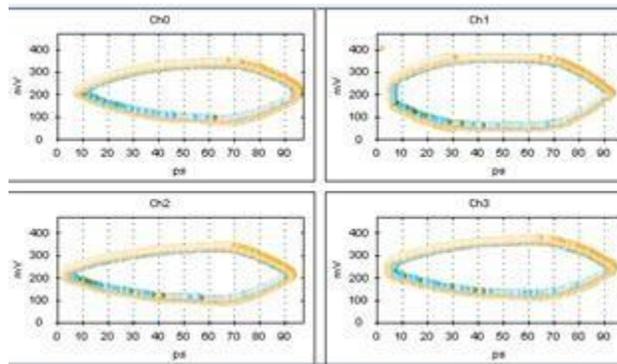


Figure 26: 4 Channels Eye Contour

Mask test

Masks typically represent an area in the eye opening that you want to ensure unit intervals do not fall within.

The mask test is highly efficient since it quantifies both time and amplitude parameters in one measurement.

The user should check the checkbox of the MASK to view the failing points, after specifying the X and Y values of every point in the mask.

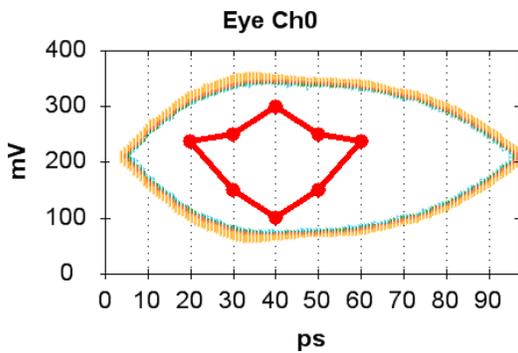


Figure 27: Eye Mask

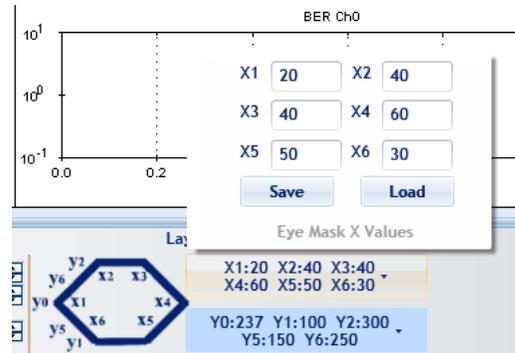


Figure 28: X and Y values

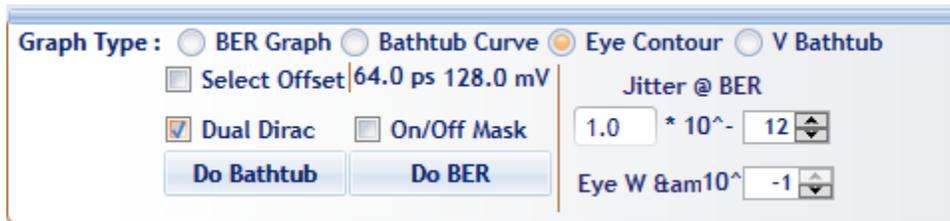


Figure 29: Check Mask

Vertical Bathtub

The V Bathtub allows the user to get the vertical Bathtub of a specific channel.

The value entered in the textbox must be in ps, and according to the estimated time 2 s, the curve will be drawn. Also the deep eye height can be entered to get the BER level.

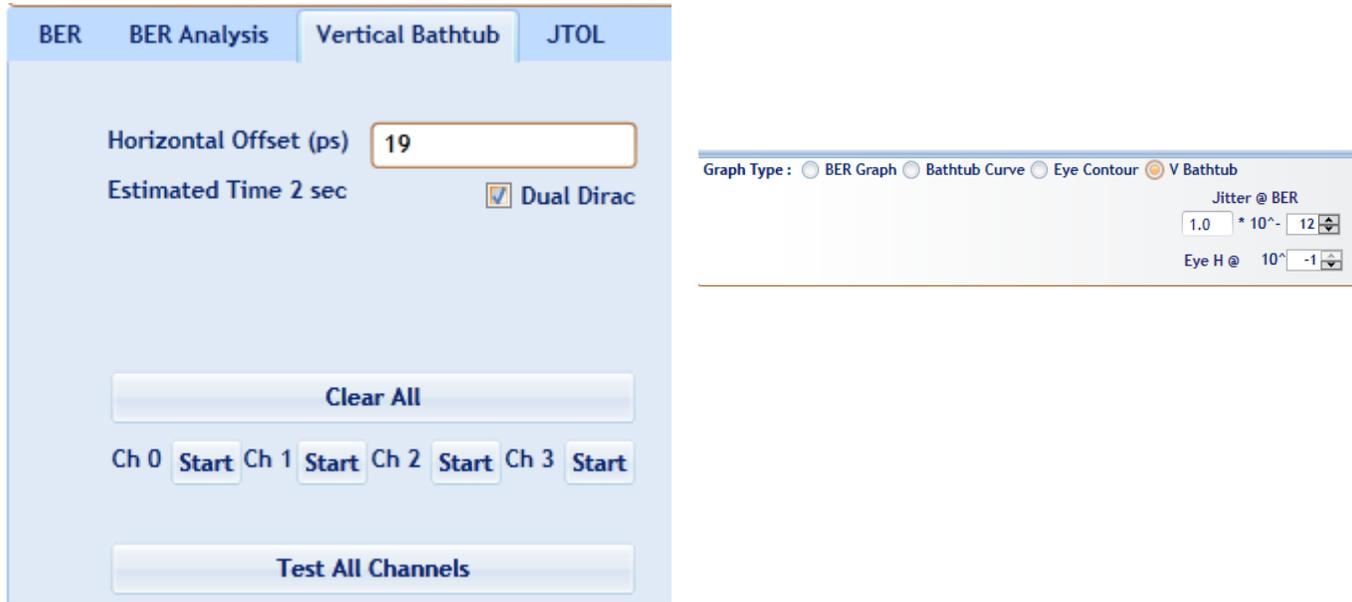
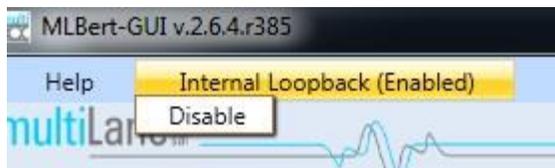


Figure 30: Vertical Bathtub

Internal Loopback

When the GUI runs, the internal loopback is disabled. The user should enable it if he wants to make the TX and RX channels irrelevant.



After enabling the internal loopback, the RX will be connected to the TX in the 4 channels, and the user will not be able to make TX generation anymore.

Log file System

In the ML4039 BERT there is a log file system, where every exception handled or unhandled by the GUI will be saved. After the first run, the GUI creates a file in the main directory/exception log, and saves all the existed exceptions. In case the user had a problem with software, he can send the exception file to our team.

Note: the exception file will be deleted automatically after every 1 week of work.

How to connect this instrument

This session covers the connection options of the instrument, addressing the following topic:

- **ML4039** BERT Fast Ethernet / USB Connections method.

NOTE. This release supports Ethernet connection for the software applications (note that the IP¹ should be in the same range of the network).

Connecting Through an Ethernet cable

To establish an Ethernet connection between the **ML4039** panel and the PC, connect an Ethernet **straight** cable between the panel and the Router or Switch, and sure you can connect your PC to the router via cable or wireless. The device can be pinged to verify that a connection has been established.

Make sure to have the correct IP address

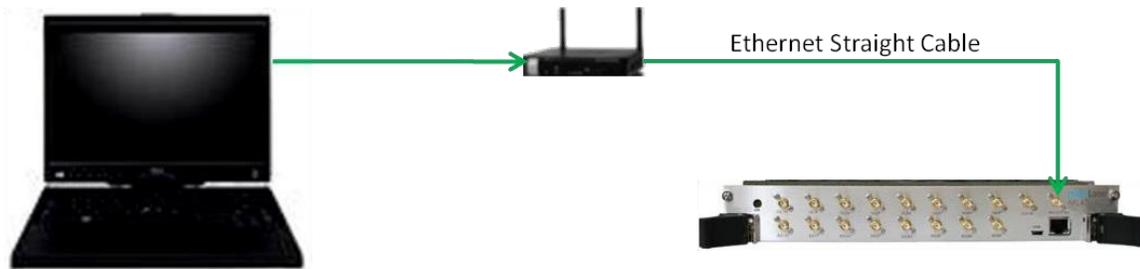


Figure 31: **ML4039** connected to PC via Ethernet

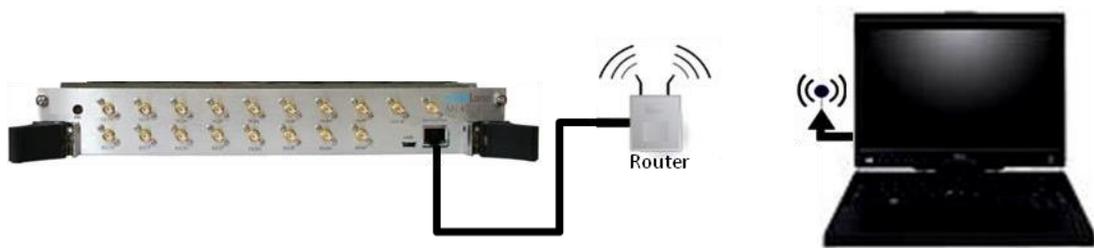


Figure 32: **ML4039** connected to PC via Wireless

¹[http:// en.wikipedia.org/wiki/IP_address](http://en.wikipedia.org/wiki/IP_address)

Connecting Through USB cables

Connect a USB cable between the panel and the PC.

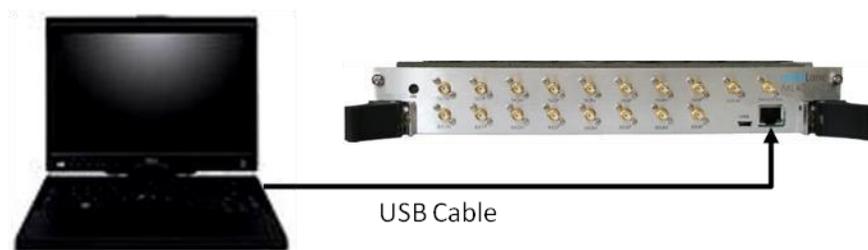


Figure 33: ML4039 with USB connection

USB Driver Installation

During the MultiLane’s software installation, the USB drivers of a specific instrument should normally be installed automatically. If for any reason this step couldn’t be completed, or any error window similar to the below picture appears, it is recommended to install the USB drivers manually, after you press on cancel and continue the installation proces.

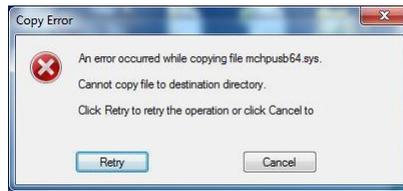


Figure 34: USB Driver Not Installed

USB software drivers’ names:

- **ML4039 USB driver**

The following instructions are applicable for a manual USB driver installation using Windows XP, Windows 7 and 8.

- Power on the instrument.
- Plug-in the USB cable into the PC and connect it to the panel; refer to the section [Connect through USB cables](#).

USB Driver Installation on Windows XP, Windows 7 platforms

- Ignore the messages *new hardware found* or *driver software not successfully installed* by pressing **cancel** or **close**.
- Go to the device manager via a right click on **My Computer**:
 - Click on **Manage**.
 - Click on **Device Manager**.
- Right click on the top level tab (Here multilane-PC) and select “**Scan for hardware changes**”.

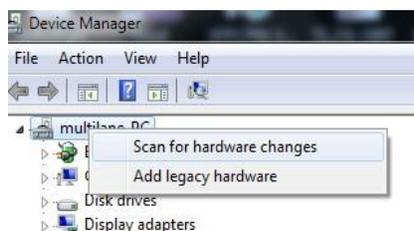


Figure 35: Scan for Hardware Changes

- A message appears stating: **“Scanning Plug and Play compliant hardware”**.



Figure 36: Scanning for Plugs

- In the **Other Devices** tab, the **ML4039 USB Device** description appears.
- In the **Other Devices** tab, right-click on the **ML4039 USB Device** and select **“Update Driver Software”**
- A dialog box appears asking for the method to search for the driver software. Select **“Browse my computer for driver software”**.
- A dialog box appears asking for the Driver software path. Enter the path and click **“Next”**.
- A security dialog box appears, select **“Install this driver software anyway”**.
- The PC commences Driver software installation.
 - A Windows message appears (after some time) saying that you have successfully updated your driver software.
- Press close.
- In the Device Manager, a new tab appears named **MultiLane SAL Devices**. Expanding it reveals **“MultiLane SAL ML4039 USB Device”**.
- You are now connected via USB and you can control the instrument.

USB Driver Installation on Windows 8+ platforms:

- Select **“Settings”** for the right side menu, then **“Change PC settings”** 1.2. Under the **“General”** tab, scroll down to **“Advanced startup”** and click on **“Restart now”**
- Select **“Troubleshoot/Advanced options/Startup settings/Restart”** 1.4. Press **“F7”** for the **“(7) Disable driver signature enforcement”**
- Install the MCHPUSB driver manually from MCHPUSB.inf (**“Install this driver software anyway”**)
- Control Panel
 - Open **“Device manager”** from the **“Control panel”** .Right click the unrecognized device and select **“Update driver software”** .Select **“Browse my computer for driver software”** .Select **“Let me pick from a list of device drivers on my computer”** . Select **“Custom USB device”** . Select the corresponding model (Microchip Custom USB Device)

Firmware Upgrade

The PIC32 Bootloader program automatically runs when the ML4039 GUI detects incorrect or outdated firmware. The following software is needed to load the firmware:

- ML Configuration Gui

Instructions to upgrade the Firmware

1. When connecting to an instrument with outdated/incorrect firmware, the board LEDs 1 and 2 start blinking and Bootloader Software pops up automatically (Figure 37)

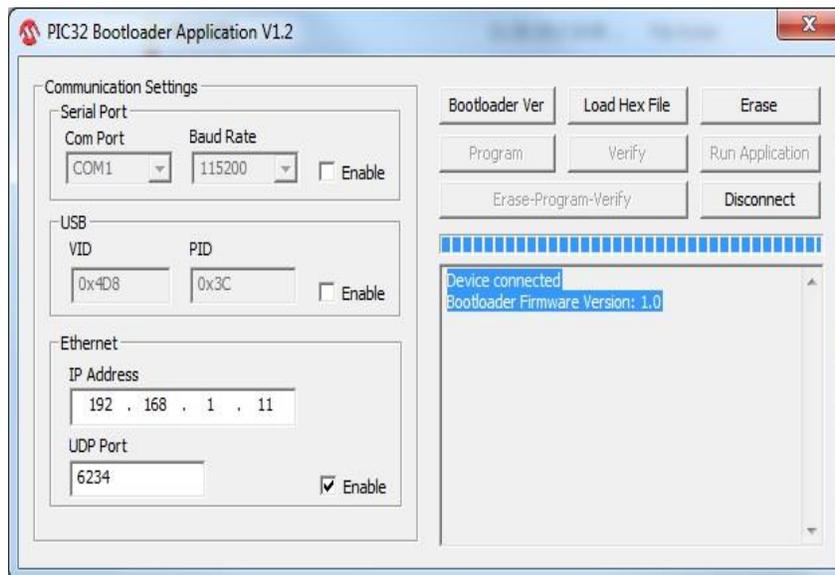


Figure 37: Bootloader Software

2. User has the option for loading the new firmware.
3. Set IP at 192.168.1.11 and UDP port at 6234, press on “Enable”, check box in the Ethernet Tab and then press “Connect” button. If connection is successful, the software will display “Device connected Bootloader Firmware Version: 2.0”
4. Otherwise, attach a USB cable to the board and press “Enable” check box in the USB tab of the GUI then press on “Connect” as shown in Figure 38.

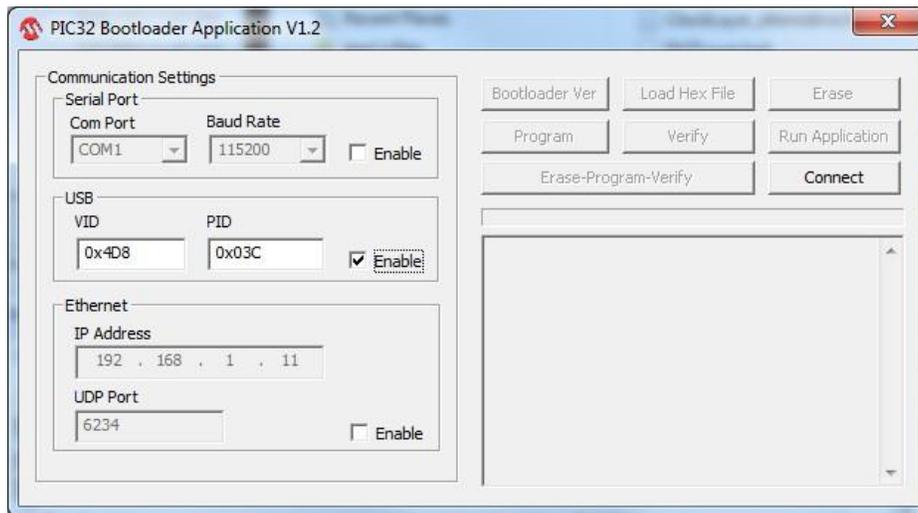


Figure 38: Connect Bootloader Software

5. Press “Load Hex File” then load the new ML4039 firmware and press “Open”(Figure 39). The path of the firmware file is C:/Program files/Multilane SAL/ML BERT/FWLoad.

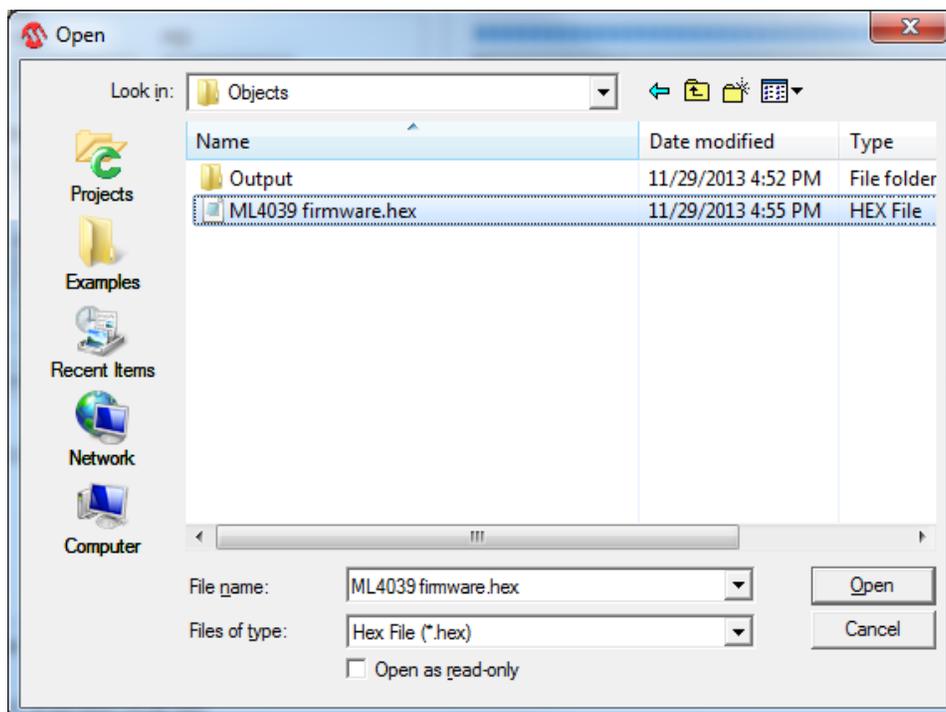


Figure 39: Select Hex File

6. Press “Erase-Program-Verify” button. Successful loading will be indicated by the bootloader software similar to Figure 40.

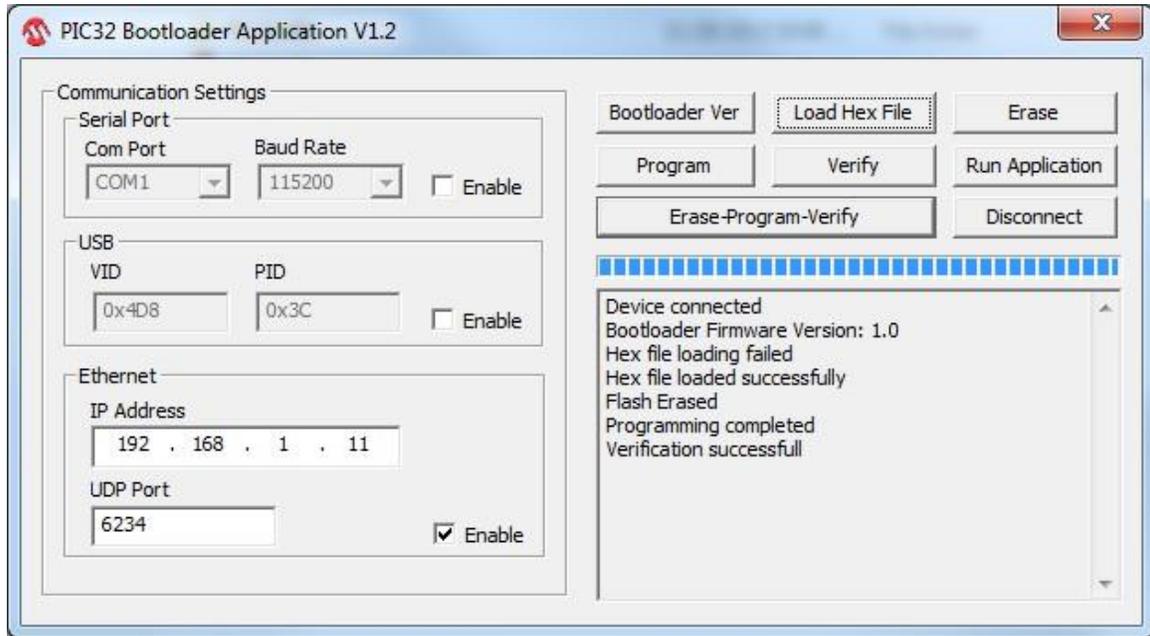


Figure 40: Erase Program Verify

7. power cycle the ML4039
8. ML4039 is now ready for normal operation

In case the user lost the old IP (when upgrading the firmware or when changing the IP) or when the IP is mistakenly erased, he can always put a jumper and power cycle the board, this will initiate the board in the default IP which is 172.16.100.217

Related Products

For a complete transmitter/receiver test solution, MultiLane offers the following products:

- **ML4009**: single Channel BERT for low cost production testing.
- **ML4039-JIT**: 4 Channel BERT with full jitter control for receiver sensitivity and jitter tolerance testing.
- **ML4009-JIT**: Single channel with full jitter control for receiver sensitivity and jitter tolerance testing in a standalone metal box.

Ordering Information

Order No.	Description
ML4039	4 Channels 30 Gbps BERT
ML4039-HV	4 Channels 30 Gbps BERT with High Voltage output
ML4039-JIT	4 Channels 30 Gbps BERT with Jitter Generation
ML4039-3W	3-Year Warranty
ML4000	6U cPCI Chassis
	<ul style="list-style-type: none"> • Please select <u>cPCI</u> form factor or <u>ATE (5" x 6.5")</u> form factor. • Standard Warranty - 1 Year
<p><i>For more information on this or other products, contact Multilane sales team by email at sales@multilaneinc.com</i></p>	

Table 2: Order Information

For more information on this or other products contact MultiLane sales team by email at sales@multilaneinc.com.

Manual Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 2.1: March 24rd, 2014; First publication of this document, preliminary revision.

Revision 2.2: March 25th, 2014; Second Publication of this document, updates Rate range.

Revision 2.3: April 30th, 2014; Third Publication of this document, updates GUI Layout.

Revision 2.4: May 6th, 2014; Fourth Publication of this document, grammar/content revisions.

Revision 2.5: December 16th, 2014

Revision 2.6: February 10th, 2015

Revision 2.7: June 15th, 2016

Revision 2.8: January 3rd, 2017

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